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uATX(243.84mm X 203.2mm)

CPU:

INTEL -Clarkdale/Lynnfied LGA 1156

System Chipset:

INTEL-IBEXPEAK PCH

OnBoard Chipset:

Clock Gen:Realtek RTM875N-632

HD Audio Codec:ALC887-VD-GR

LAN:RTL8111E 10/100/1000

IO: Fintek F71858AD

Flash ROM: 32 Mb SPI (CHIP)

Main Memory:

DDRIII (1066/1333MHz) * 2 (Dual Channel)

Expansion Slots:

PCI Express (X16) Slot * 1

PCI Express (X1) Slot * 2

PWM:

Controller:NCP5395 3-Phase -- 95W

Other:

SATA(SATA2-300MB/s) *4

USB2.0 *10 (Rear*4 / Front*4)

USB3.0*2

On BOARD BUZZER



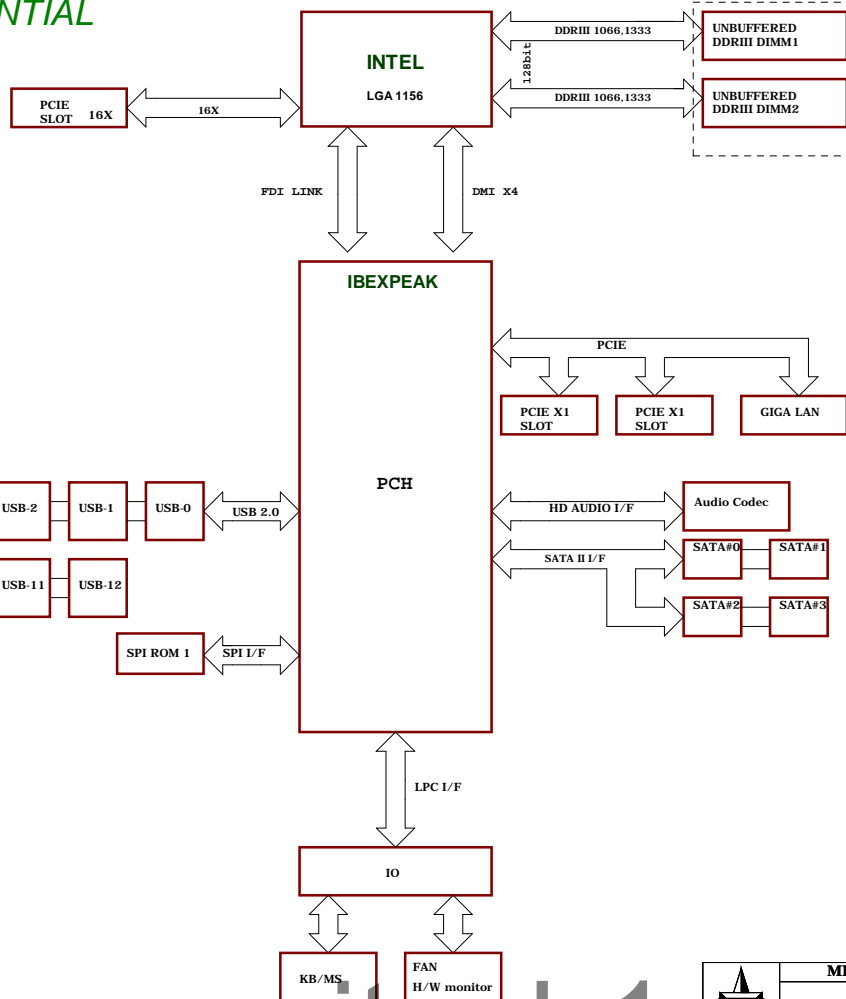
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DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 2 CH-A	10100001B	MEM_MA_CLK_H2/L2 MEM_MA_CLK_H3/L3
DIMM 1 CH-A	10100000B	MEM_MA_CLK_H0/L0 MEM_MA_CLK_H1/L1
DIMM 4 CH-B	10100011B	MEM_MB_CLK_H2/L2 MEM_MB_CLK_H3/L3
DIMM 3 CH-B	10100010B	MEM_MB_CLK_H0/L0 MEM_MB_CLK_H1/L1

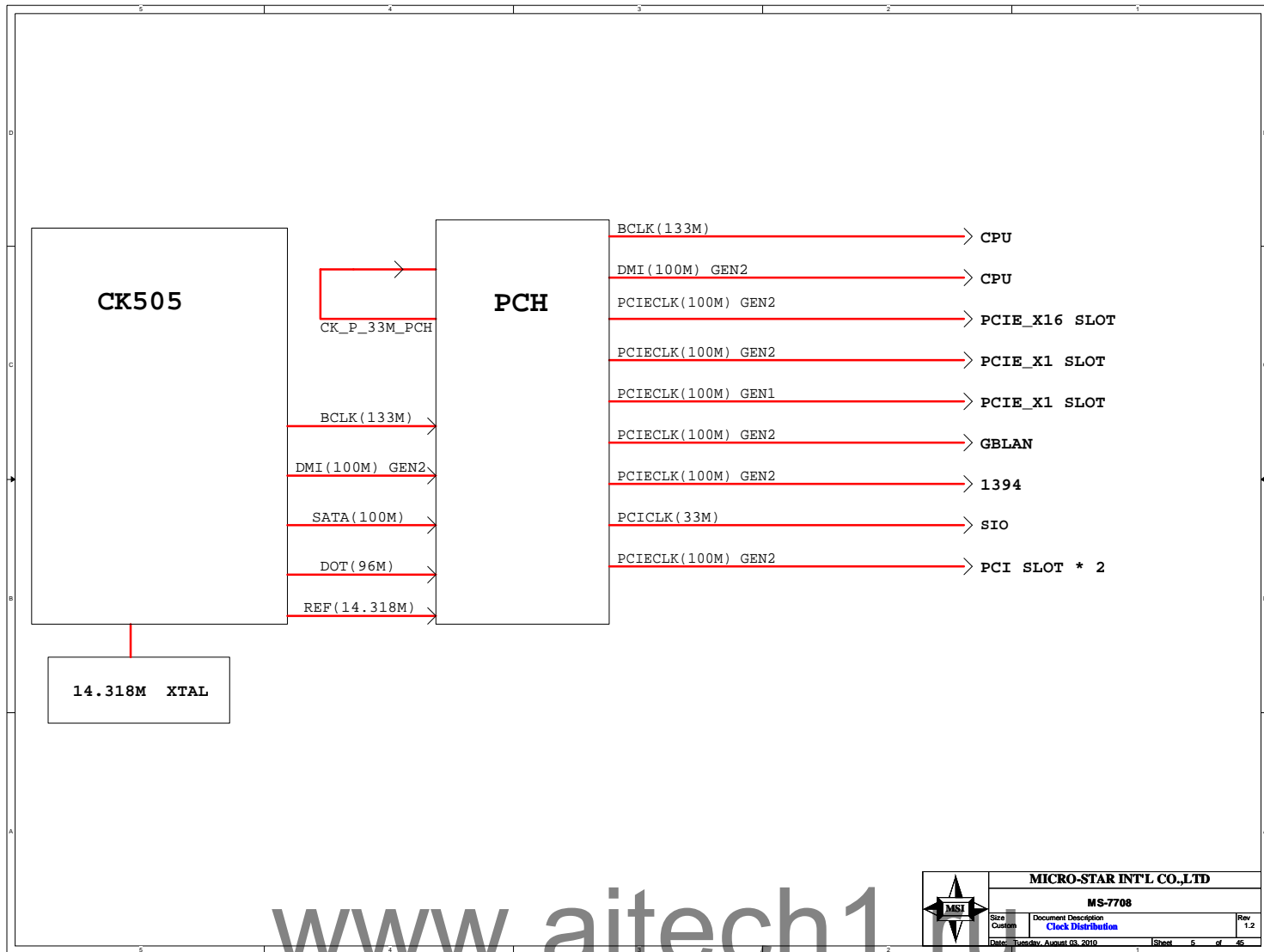
TABLE 9:
USB PORT MAPPING SUBJECT TO CHANGES

Controller	Port	Destination	max. USB Ports	Full Cap.	Over Current Protection
UHCI2, EHCI	Port 1	Internal USB, Device F15.0	255	Y	Y
	Port 2	Internal USB, Device F15.0	255	Y	Y
UHCI2, EHCI	Port 3	Internal USB, Device F15.0	255	Y	Y
	Port 4	Internal USB, Device F15.0	255	Y	Y
UHCI2, EHCI	Port 5	Internal USB	255	Y	Y
	Port 6	Internal USB	255	Y	Y
UHCI2, EHCI	Port 7	Internal USB	255	Y	Y
	Port 8	Internal USB	255	Y	Y
UHCI2, EHCI	Port 9	Internal USB	255	Y	Y
	Port 10	Internal USB	255	Y	Y
UHCI2, EHCI	Port 11	Internal USB	255	Y	Y
	Port 12	Internal USB	255	Y	Y
UHCI2, EHCI	Port 13	Internal USB	255	Y	Y
	Port 14	Internal USB	255	Y	Y
UHCI2, EHCI	Port 15	Internal USB	255	Y	Y
	Port 16	Internal USB	255	Y	Y
UHCI2, EHCI	Port 17	Internal USB	255	Y	Y
	Port 18	Internal USB	255	Y	Y
UHCI2, EHCI	Port 19	Internal USB	255	Y	Y
	Port 20	Internal USB	255	Y	Y

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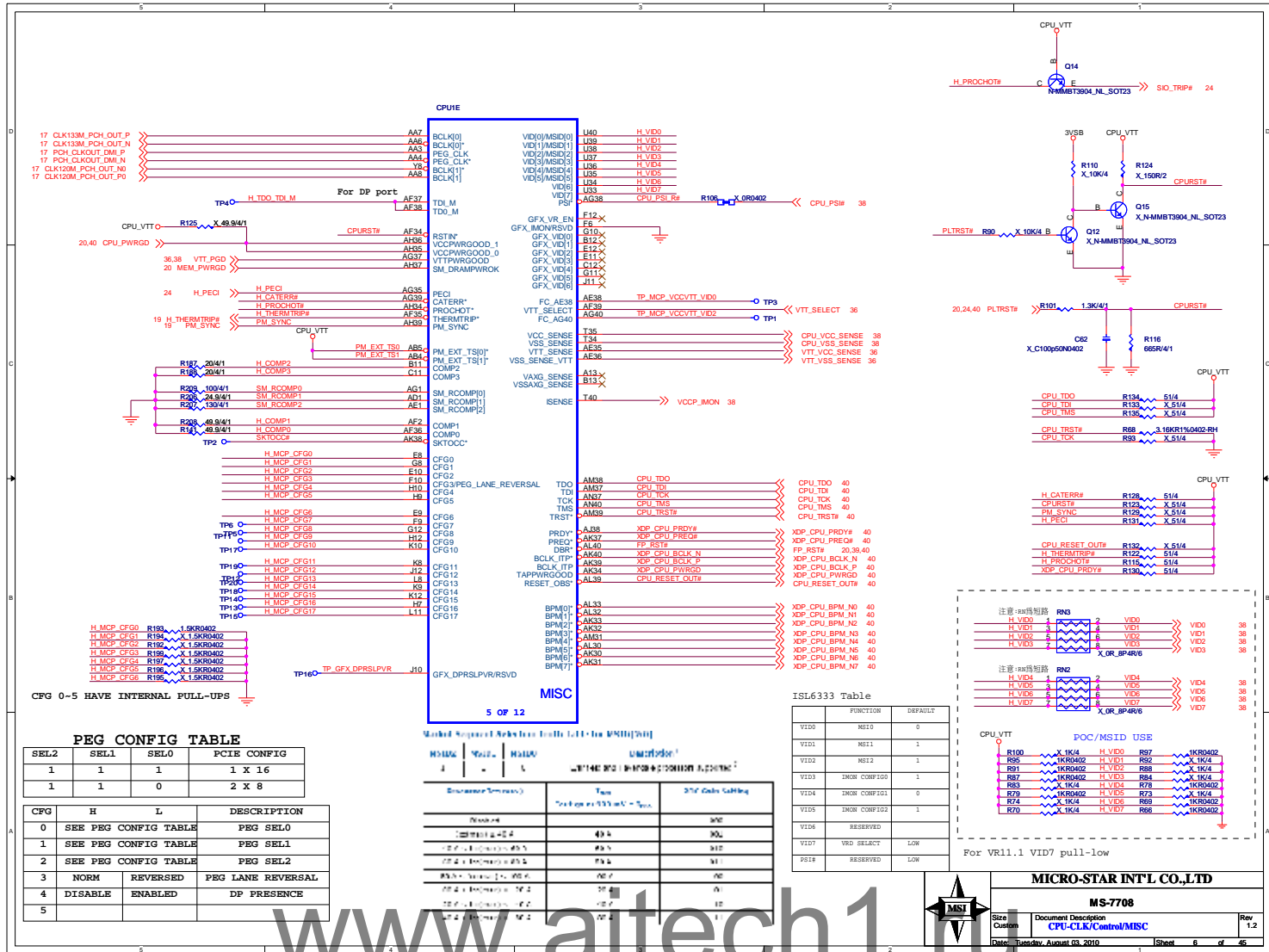
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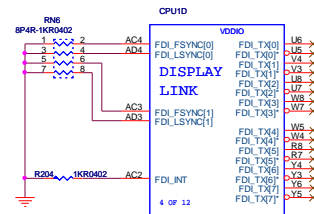
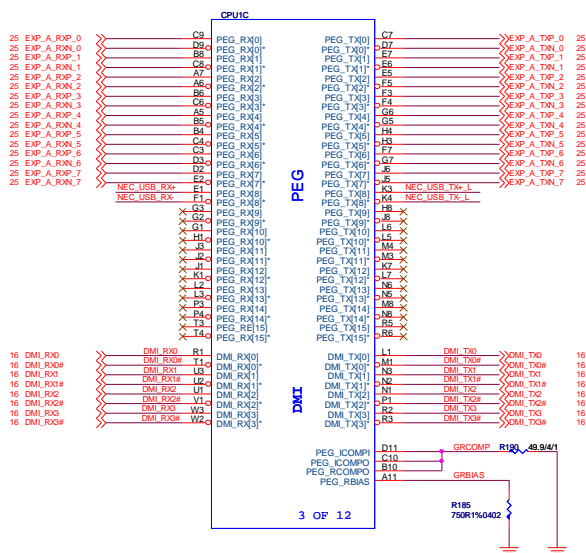
Name	Net Name	Type	Tolerance	Recommendations
GP100	BM_BUSY#	GP100	I/O	3.3V
TACH1_GP101	GP101	GP101	I/O	3.3V
PIRQ#_N_GP102	PIRQ#	GP102	I/O	5V
PIRQ#_N_GP103	PIRQ#	GP103	I/O	5V
PIRQ#_N_GP104	PIRQ#	GP104	I/O	5V
PIRQ#_N_GP105	PIRQ#	GP105	I/O	5V
PIRQ#_N_GP106	GP106	GP106	I/O	3.3V
PIRQ#_N_GP107	GP107	GP107	I/O	3.3V
PIRQ#_N_GP108	PCH_GP108	GP108	I/O	3.3V
PIRQ#_N_GP109	MeIO2	GP109	I/O	3.3V
OC5_N_GP1010	MeIO3	GP1010	I/O	3.3V
SMBALERT#_N_GP1011	PCH_SMBALERT#	GP1011	I/O	3.3V
LAN_PHY_PWR_CTRL_GP1012	CLAR_PW	GP1012	I/O	3.3V
GP1013	GPIO_PWE#	GP1013	I/O	3.3V
OC7_N_GP1014	USB0_SMI	GP1014	I/O	3.3V
GP1015	SP1_H0LD_GP0#	GP1015	I/O	3.3V
SATA4GP_GP1016	SATA4GP_FU	GP1016	I/O	3.3V
TACH0_GP1017	GP1017	GP1017	I/O	3.3V
PCHCLKREQ3_N_GP1018	PCH_CLK#	GP1018	I/O	3.3V
SATA1GP_GP1019	SATA1GP_FU	GP1019	I/O	3.3V
PCHCLKREQ2_N_GP1020	PCH_GP20	GP1020	I/O	3.3V
SATA0GP_GP1021	SATA0GP_FU	GP1021	I/O	3.3V
SCLOCK_GP1022	SCLOCK	GP1022	I/O	3.3V
LDRQ1_N_GP1023	LDRQ1#	GP1023	I/O	3.3V
GP1024	M17985461	GP1024	I/O	3.3V
PCHCLKREQ3_N_GP1025	PCHCLKREQ#	GP1025	I/O	3.3V
PCHCLKREQ4_N_GP1026	LED_SW	GP1026	I/O	3.3V
GP1027	PCH_GP1027	GP1027	I/O	3.3V
GP1028	USB_MODE	GP1028	I/O	3.3V
SLP_LAN#_N_GP1029	SLP_LAN#	GP1029	I/O	3.3V
PCHCLKREQ3_N_GP1030	SUS_PWR_ACK	GP1030	I/O	3.3V
GP1031	GP1031	GP1031	I/O	3.3V
GP1032	SP1_WP#	GP1032	I/O	3.3V
GP1033	PCH_GP1033	GP1033	I/O	3.3V
STP_PCH_N_GP1034	STP_PCH#	GP1034	I/O	3.3V
SATACLKREQ0_N_GP1035	GP1035	GP1035	I/O	3.3V
SATA2GP_GP1036	SATA2GP_FU	GP1036	I/O	3.3V
SATA3GP_GP1037	SATA3GP_FU	GP1037	I/O	3.3V
SL0AD_GP1038	PCH_GP1038	GP1038	I/O	3.3V
SATA0OUT#_N_GP1039	PCH_GP1039	GP1039	I/O	3.3V
OC4_N_GP1041	MeIO1	GP1041	I/O	3.3V
PCHCLKREQ3_N_GP1044	PCH_GP144	GP1044	I/O	3.3V
PCHCLKREQ4_N_GP1045	PCH_GP145	GP1045	I/O	3.3V
PCHCLKREQ7_N_GP1046	PCH_GP146	GP1046	I/O	3.3V
P8A_CLKREQ_N_GP1047	PCH_GP147	GP1047	I/O	3.3V
SATA0OUT#_N_GP1048	PCH_GP1048	GP1048	I/O	3.3V
SATA5GP_GP1049	SATA5GP_FU	GP1049	I/O	3.3V
REQ1_N_GP1050	P8Q#1	GP1050	I/O	5.5V
GNT1_N_GP1051	PCHNT#1	GP1051	I/O	3.3V
REQ2_N_GP1052	P8Q#2	GP1052	I/O	5.5V
GNT2_N_GP1053	PCHNT#2	GP1053	I/O	3.3V
REQ3_N_GP1054	P8Q#3	GP1054	I/O	3.3V
GNT3_N_GP1055	PCHNT#3	GP1055	I/O	3.3V
P8A_CLKREQ_N_GP1056	PCH_GP156	GP1056	I/O	3.3V
TRM_Fp_GP1057	EN_NEC_FW	GP1057	I/O	3.3V
SMCLK_GP1058	PCH_SMCLK	GP1058	I/O	3.3V
CLK_CPG_SK12_SMBALERT_N_GP1060	PCH_SMBALERT#	GP1060	I/O	3.3V
SUS_STAT#_N_GP1061	M17942862	GP1061	I/O	3.3V
SUSCLK_GP1062	SUSCLK	GP1062	I/O	3.3V
SLP_S5_N_GP1063	SUSCLK	GP1063	I/O	3.3V
GP1072	GP1072	GP1072	I/O	3.3V
PCHCLKREQ0_N_GP1073	PCHCLKREQ#	GP1073	I/O	3.3V
CLK_CPG_SK12_SMBALERT_N_GP1074	PCH_SMBALERT#	GP1074	I/O	3.3V
SMBALERT_N_GP1075	PCH_SMBALERT#	GP1075	I/O	3.3V



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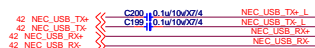
24.24 Intel® Flexible Display Interface (Intel® FDI)

Table 24-36. Intel® Flexible Display Interface Signals

Signal Name	Type	Signal Description	Connector
FDI_TX00[0]	TX	FDI_TX00[0] (TX00[0])	FDI_TX00[0]
FDI_TX00[1]	TX	FDI_TX00[1] (TX00[1])	FDI_TX00[1]
FDI_TX00[2]	TX	FDI_TX00[2] (TX00[2])	FDI_TX00[2]
FDI_TX00[3]	TX	FDI_TX00[3] (TX00[3])	FDI_TX00[3]
FDI_TX00[4]	TX	FDI_TX00[4] (TX00[4])	FDI_TX00[4]
FDI_TX00[5]	TX	FDI_TX00[5] (TX00[5])	FDI_TX00[5]
FDI_TX00[6]	TX	FDI_TX00[6] (TX00[6])	FDI_TX00[6]
FDI_TX00[7]	TX	FDI_TX00[7] (TX00[7])	FDI_TX00[7]
FDI_TX00[8]	TX	FDI_TX00[8] (TX00[8])	FDI_TX00[8]
FDI_TX00[9]	TX	FDI_TX00[9] (TX00[9])	FDI_TX00[9]
FDI_TX00[10]	TX	FDI_TX00[10] (TX00[10])	FDI_TX00[10]
FDI_TX00[11]	TX	FDI_TX00[11] (TX00[11])	FDI_TX00[11]
FDI_TX00[12]	TX	FDI_TX00[12] (TX00[12])	FDI_TX00[12]
FDI_TX00[13]	TX	FDI_TX00[13] (TX00[13])	FDI_TX00[13]
FDI_TX00[14]	TX	FDI_TX00[14] (TX00[14])	FDI_TX00[14]
FDI_TX00[15]	TX	FDI_TX00[15] (TX00[15])	FDI_TX00[15]

Table 7-6. Haswell/ Lynnfield PCI Express® and DMI Compensation Routing Guidelines

Signal Name	Width (W) / Spacing (S)	Length	Termination	Notes
PCI_EXP_B0[0]	1.5 m spacing (W) / 1.5 m spacing (S)	1.5 m	1.5 m	1.5 m
PCI_EXP_B0[1]	1.5 m spacing (W) / 1.5 m spacing (S)	1.5 m	1.5 m	1.5 m
PCI_EXP_B0[2]	1.5 m spacing (W) / 1.5 m spacing (S)	1.5 m	1.5 m	1.5 m
PCI_EXP_B0[3]	1.5 m spacing (W) / 1.5 m spacing (S)	1.5 m	1.5 m	1.5 m
PCI_EXP_B0[4]	1.5 m spacing (W) / 1.5 m spacing (S)	1.5 m	1.5 m	1.5 m
PCI_EXP_B0[5]	1.5 m spacing (W) / 1.5 m spacing (S)	1.5 m	1.5 m	1.5 m
PCI_EXP_B0[6]	1.5 m spacing (W) / 1.5 m spacing (S)	1.5 m	1.5 m	1.5 m
PCI_EXP_B0[7]	1.5 m spacing (W) / 1.5 m spacing (S)	1.5 m	1.5 m	1.5 m
PCI_EXP_B0[8]	1.5 m spacing (W) / 1.5 m spacing (S)	1.5 m	1.5 m	1.5 m
PCI_EXP_B0[9]	1.5 m spacing (W) / 1.5 m spacing (S)	1.5 m	1.5 m	1.5 m
PCI_EXP_B0[10]	1.5 m spacing (W) / 1.5 m spacing (S)	1.5 m	1.5 m	1.5 m
PCI_EXP_B0[11]	1.5 m spacing (W) / 1.5 m spacing (S)	1.5 m	1.5 m	1.5 m
PCI_EXP_B0[12]	1.5 m spacing (W) / 1.5 m spacing (S)	1.5 m	1.5 m	1.5 m
PCI_EXP_B0[13]	1.5 m spacing (W) / 1.5 m spacing (S)	1.5 m	1.5 m	1.5 m
PCI_EXP_B0[14]	1.5 m spacing (W) / 1.5 m spacing (S)	1.5 m	1.5 m	1.5 m
PCI_EXP_B0[15]	1.5 m spacing (W) / 1.5 m spacing (S)	1.5 m	1.5 m	1.5 m

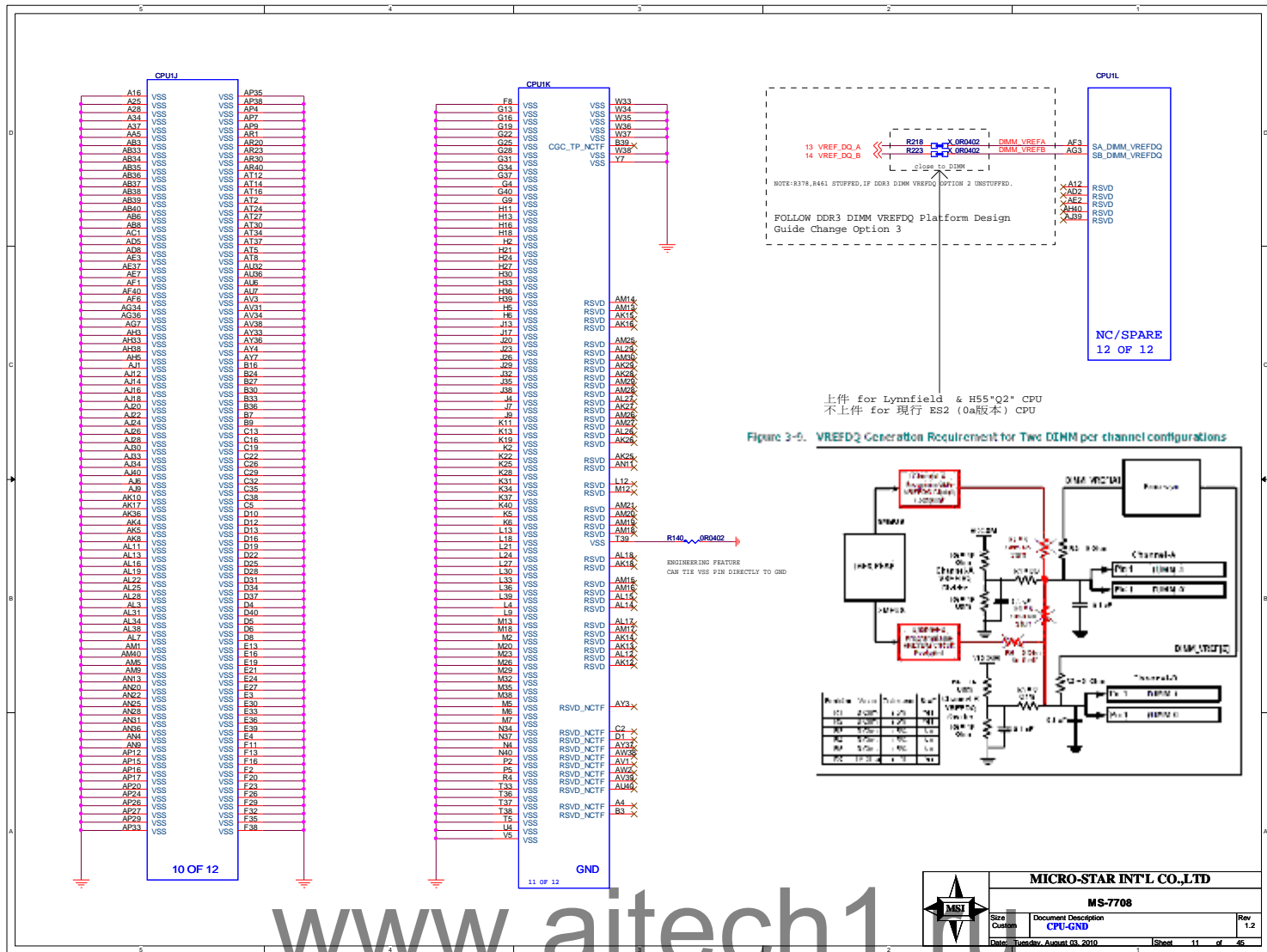


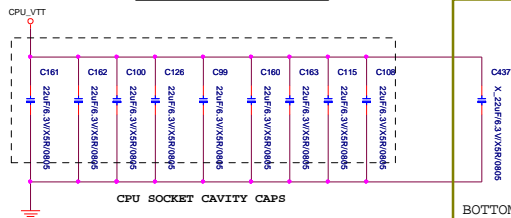
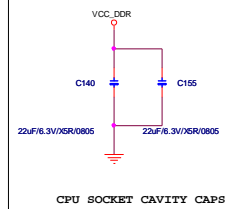
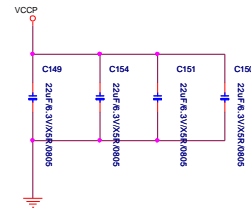
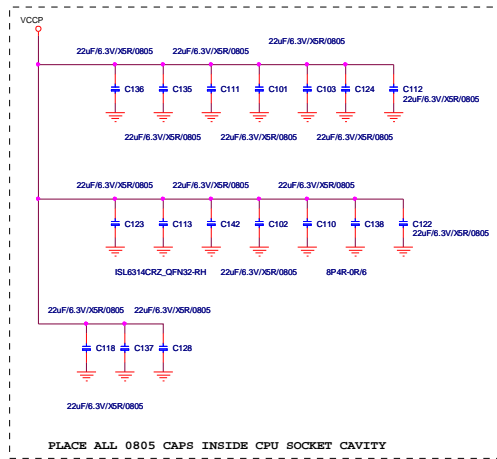
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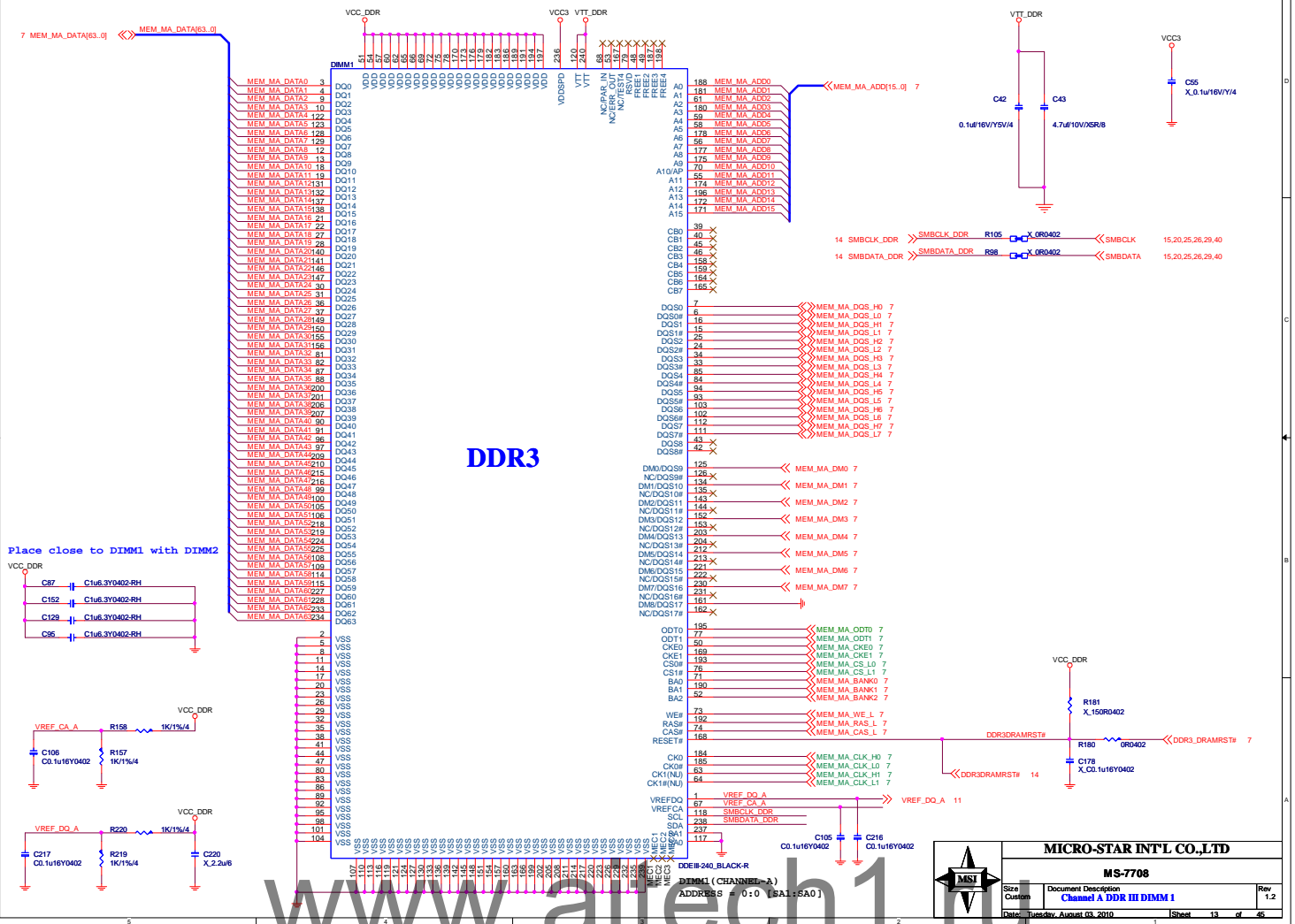
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DDRIII DIMM_A1

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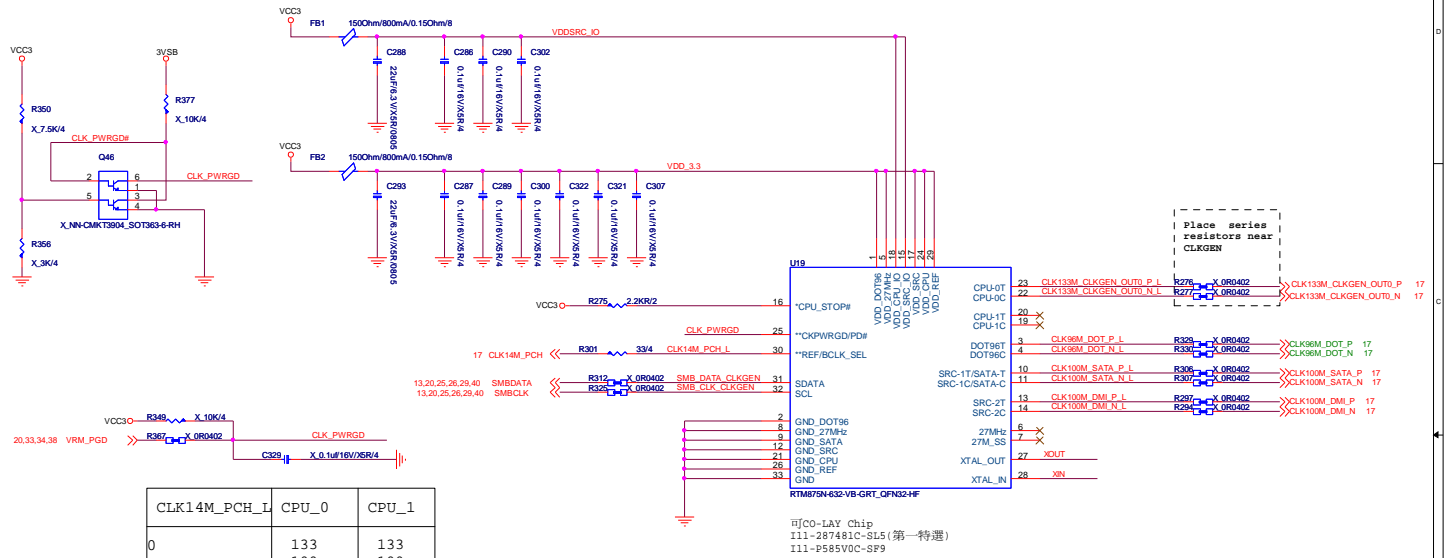
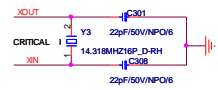
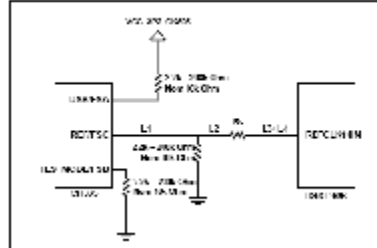
CLOCK Gen / RTM875N-632

Figure 9: L8 REFCLK Topology from C4305 to Base-Pack with DCUK Frequency Strapping



CLOCK EMI CAPS: DEFAULT EMPTY

CLK14M_PCH_L	CPU_0	CPU_1
0	133	133
1 (0.7~1.5V)	100	100

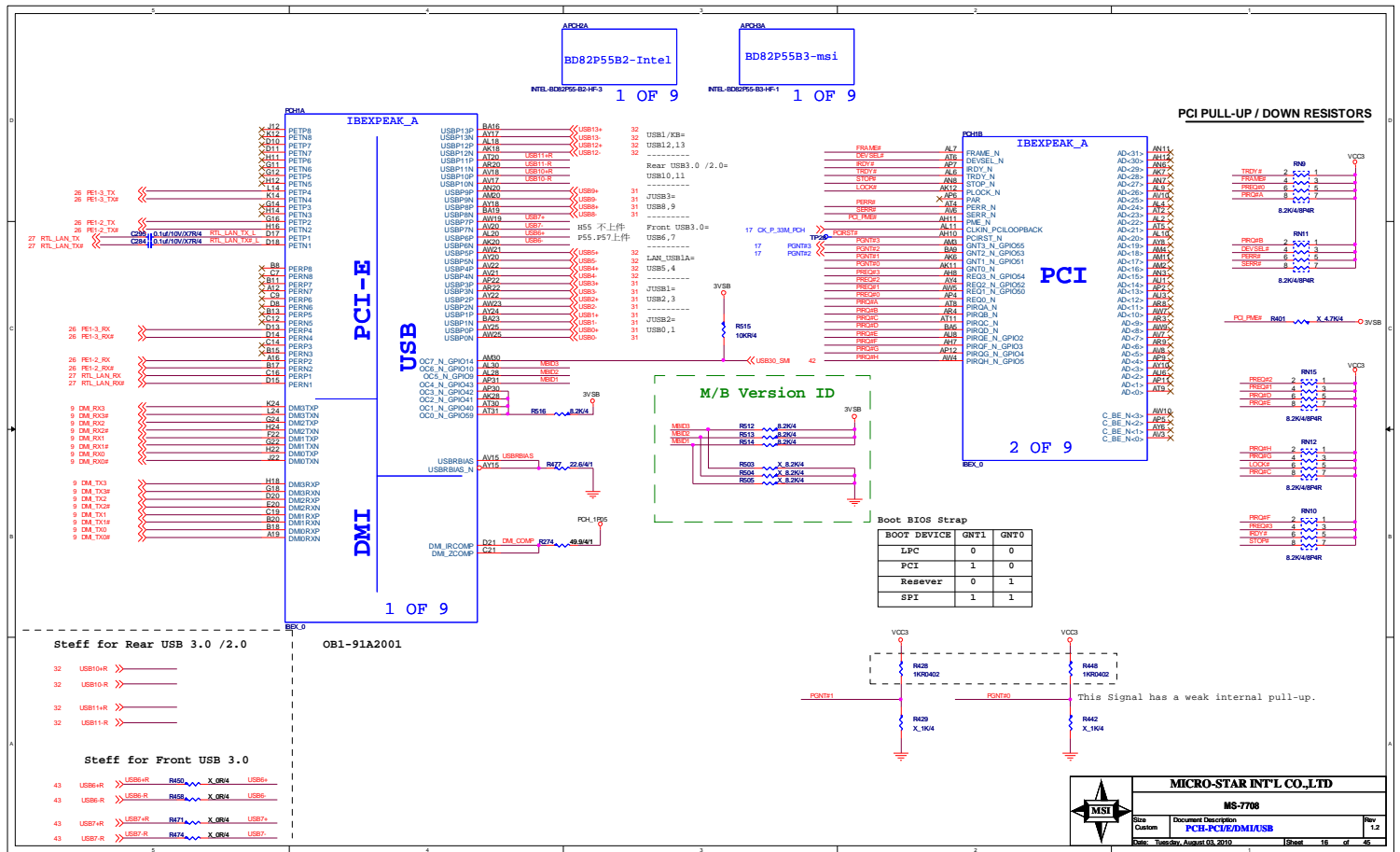
CLK14M PCH L C319 X_10pF/25V/N



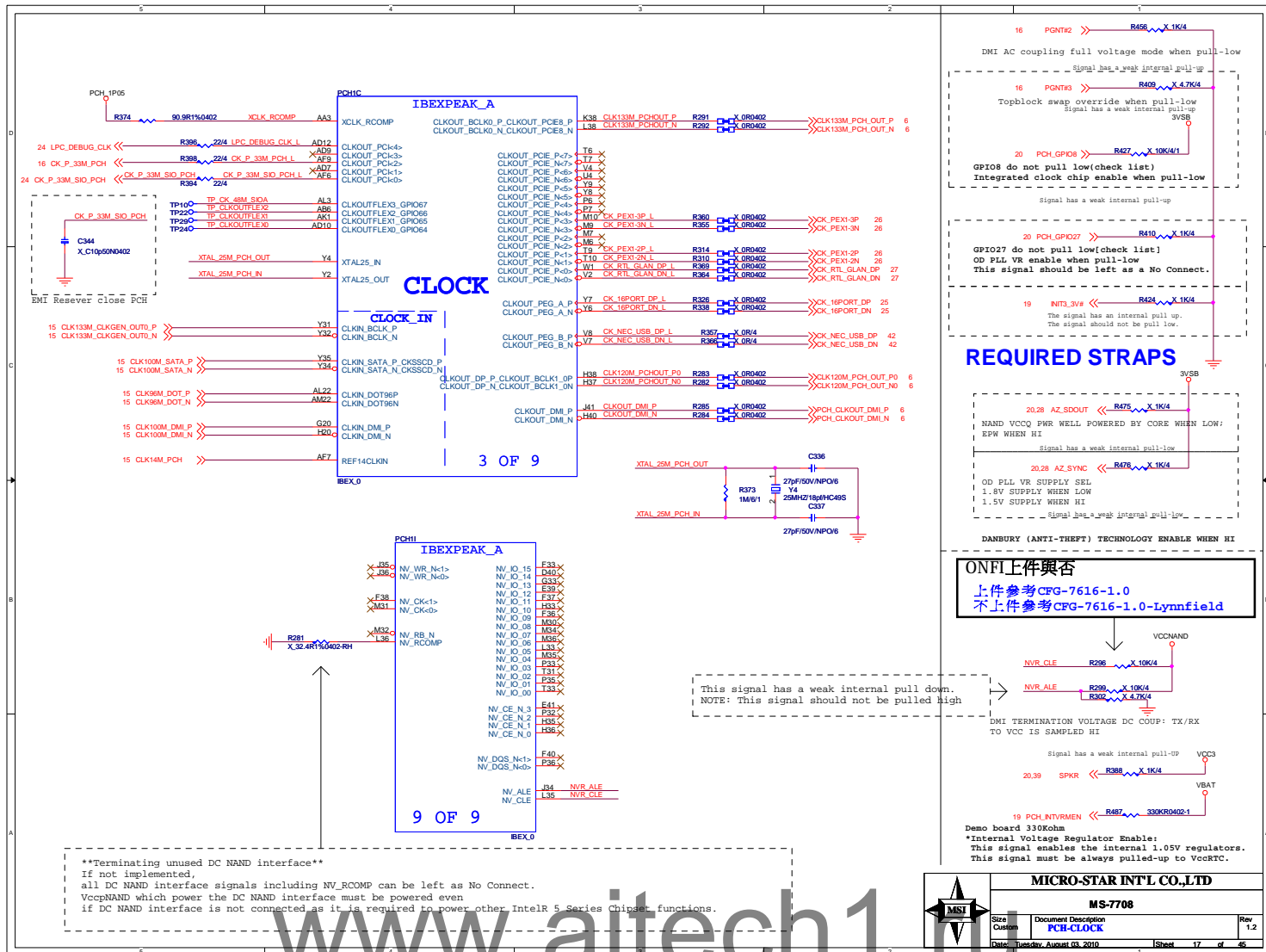
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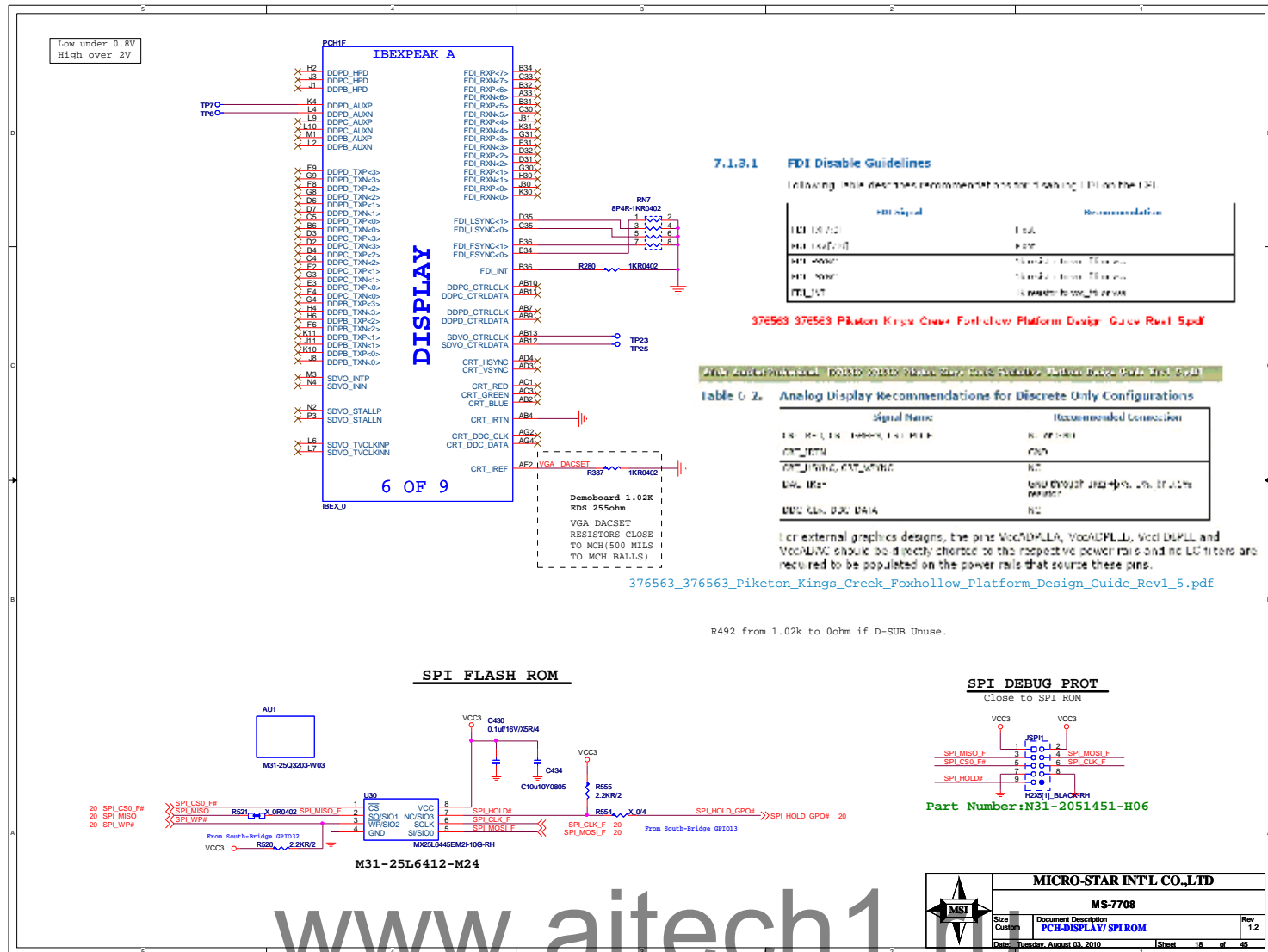
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7.1.3.1 FDI Disable Guidelines

Following table describes recommended connections for disabling FDI on the FSI.

FDI Signal	Recommendation
FDI_16/12	1.5k
FDI_16/10	1.5k
FDI_16/07	1.5k or 10k
FDI_16/06	1.5k or 10k
FDI_16/05	1.5k or 10k

376563_376563_Piketon_Kings_Creek_Foxhollow_Platform_Design_Guide_Rev1.5.pdf

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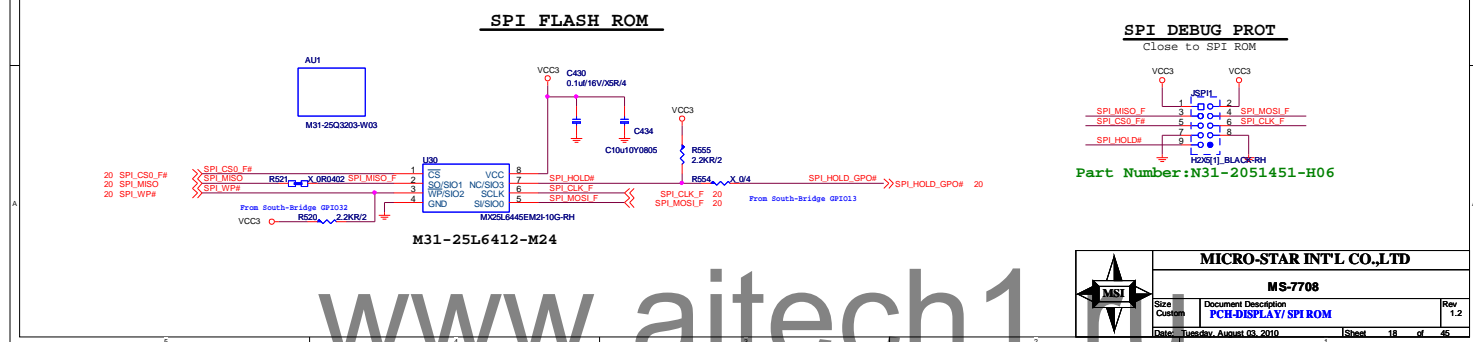
Table 6.2. Analog Display Recommendations for Discrete Only Configurations

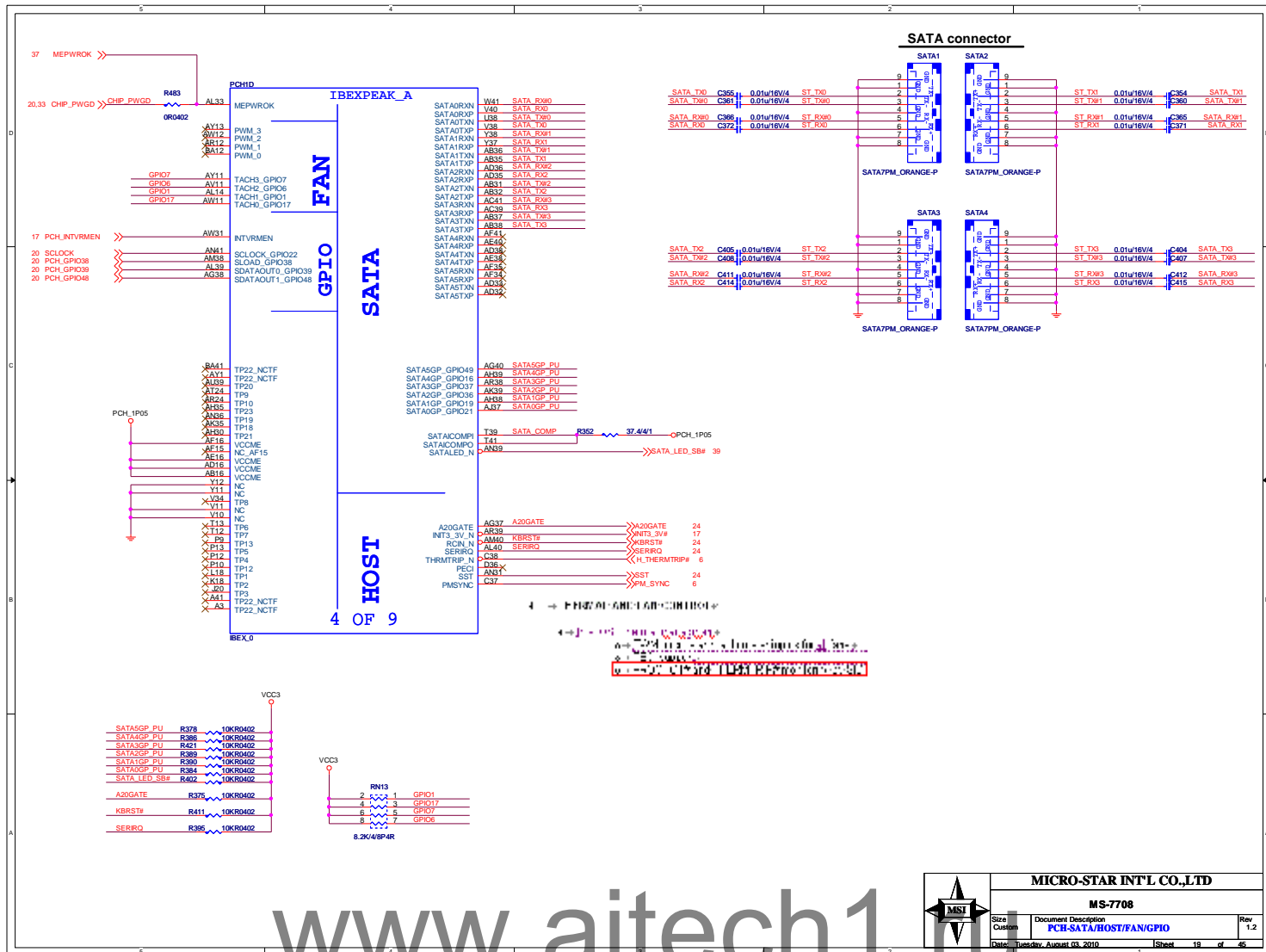
Signal Name	Recommended Connection
FDI_16/12, FDI_16/10, FDI_16/07	1.5k
FDI_16/06, FDI_16/05	1.5k
FDI_16/04, FDI_16/03	1.5k or 10k
FDI_16/02, FDI_16/01	1.5k or 10k
FDI_16/00, FDI_16/01	1.5k or 10k

For external graphics designs, the pins VccADP4A, VccADP4B, VccADP4C and VccADP4D should be directly connected to the respective power rails and no LC filters are required to be populated on the power rails that source these pins.

376563_376563_Piketon_Kings_Creek_Foxhollow_Platform_Design_Guide_Rev1.5.pdf

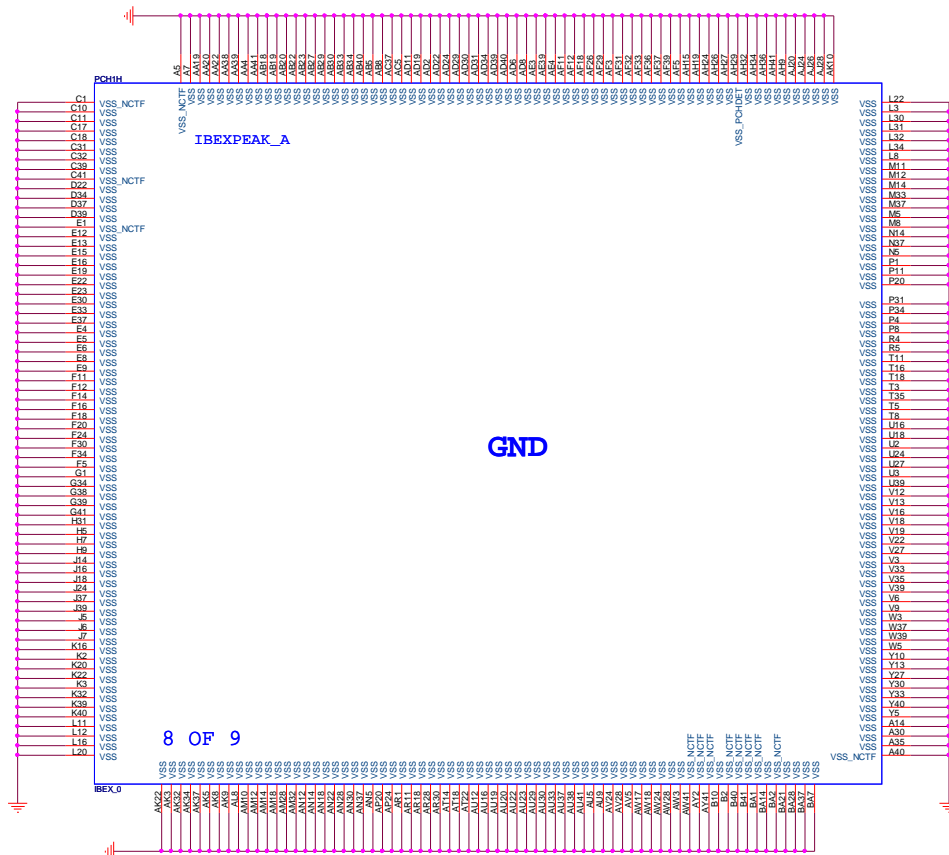
R492 from 1.02k to 0ohm if D-SUB Unuse.





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Trace width > 200 mils

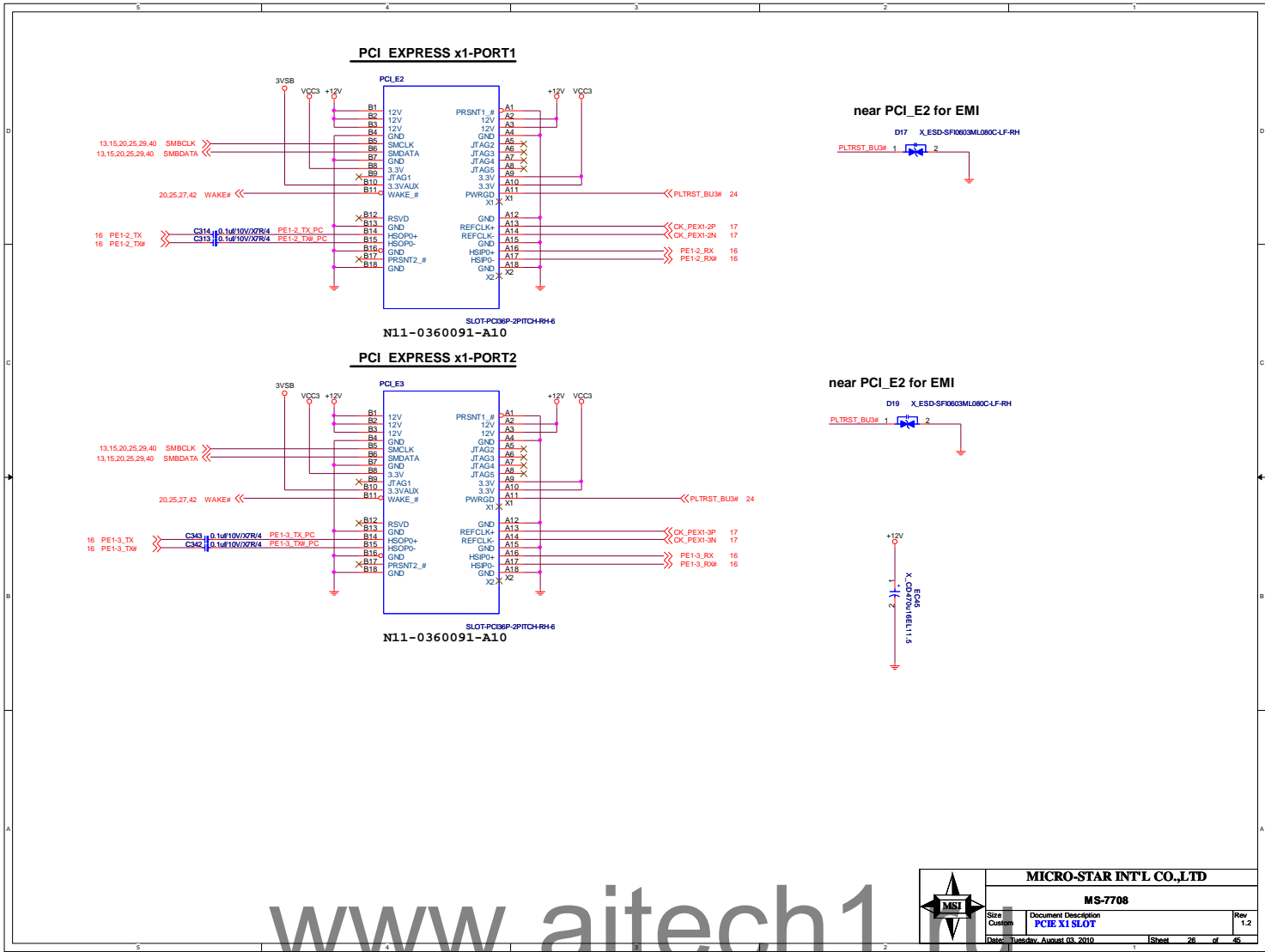


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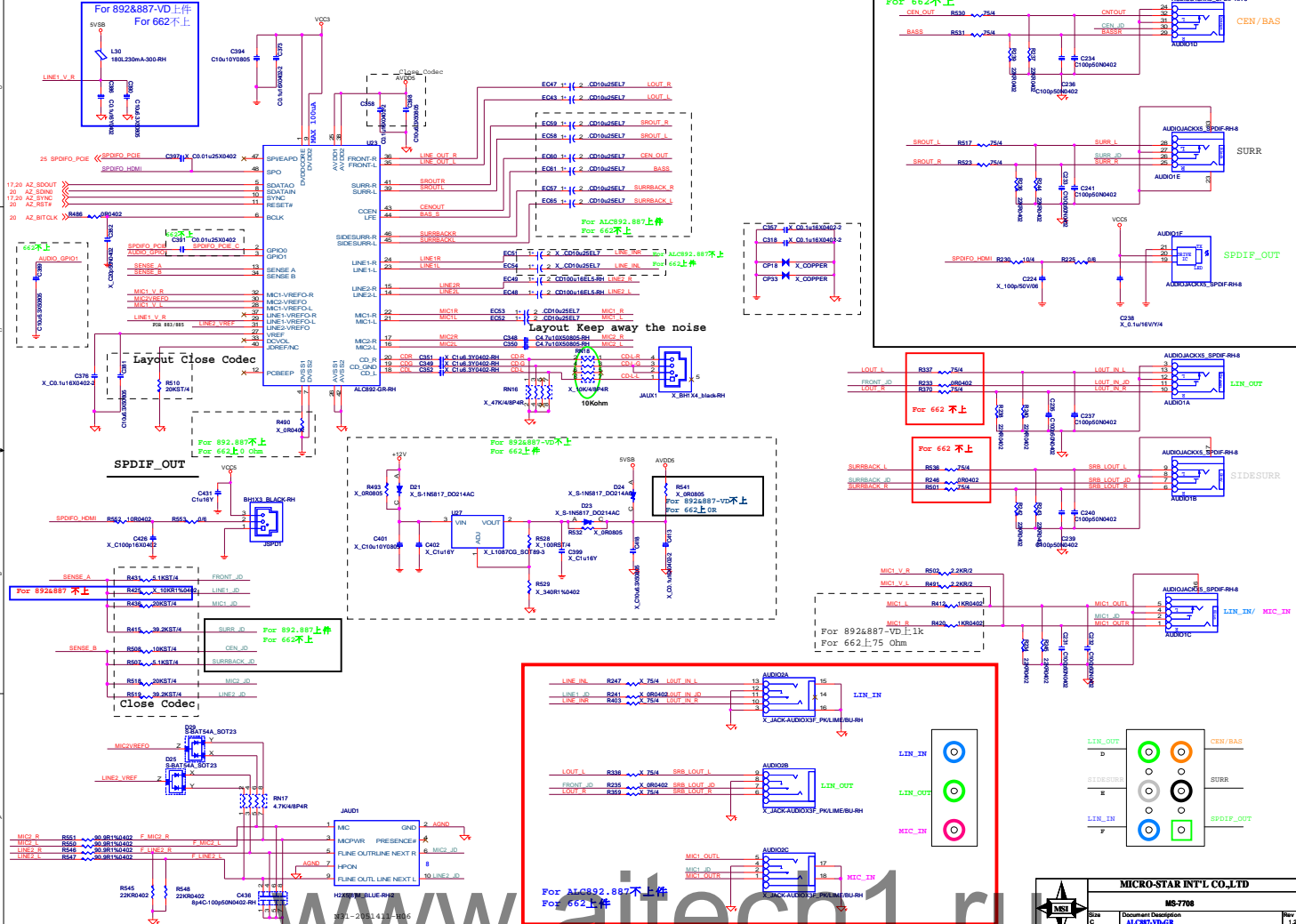


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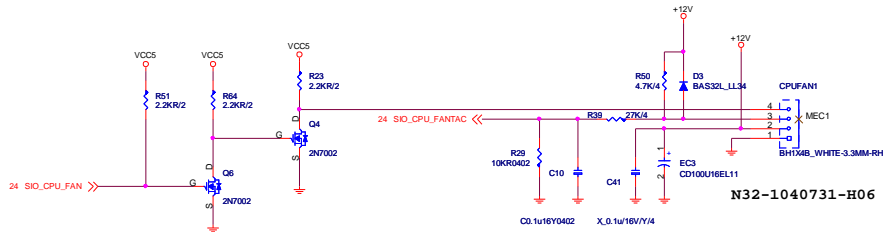
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ALC887-VD-GR



FAN-COUNTROL CIRCUIT



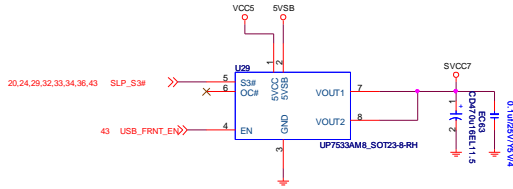
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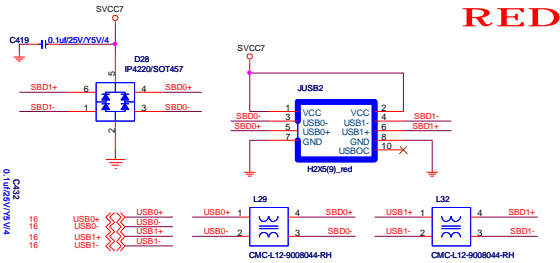
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FRONT POWER CONTROL

POWER CIRCUIT FOR USB PORT 0, 1



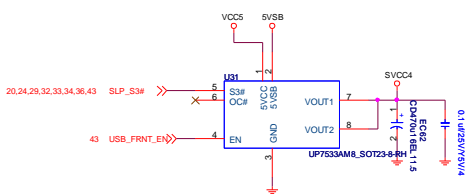
FRONT PANEL USB CONNECTOR FOR USB PORT 0,1



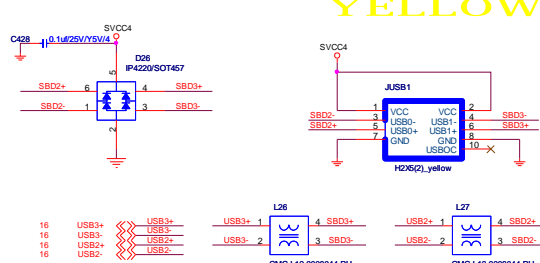
RED

NEAR USB CONNECTOR

POWER CIRCUIT FOR USB PORT 2, 3



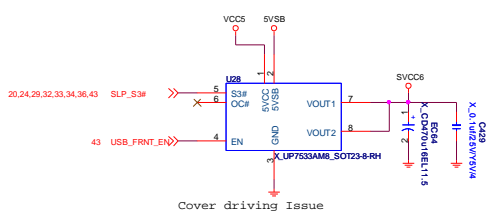
FRONT PANEL USB CONNECTOR FOR USB PORT 2,3



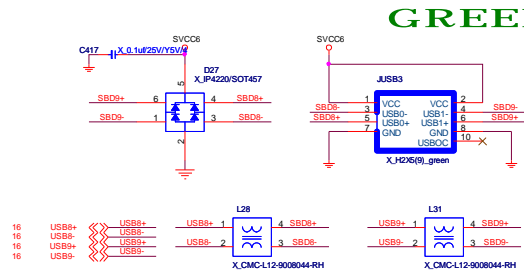
YELLOW

NEAR USB CONNECTOR

POWER CIRCUIT FOR USB PORT 8, 9



FRONT PANEL USB CONNECTOR FOR USB PORT 8, 9



GREEN

NEAR USB CONNECTOR

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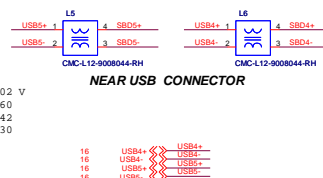
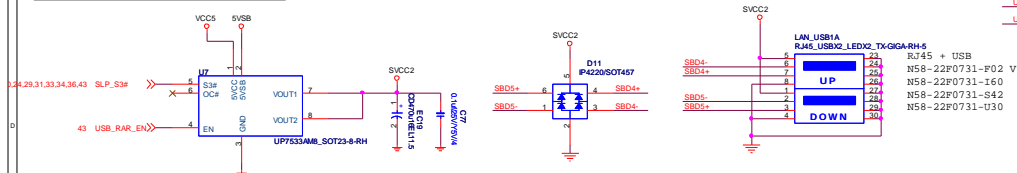
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MS-7708

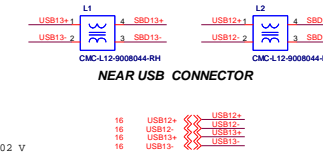
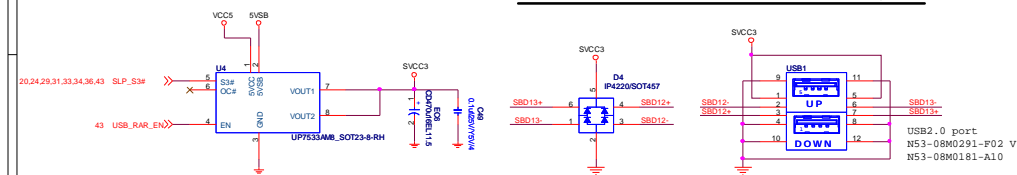
Size	Custom	Document Description	FRONT USB2.0	Rev	1.2
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REAR POWER CONTROL

REAR PANEL USB/LAN CONNECTOR FOR USB PORT 4,5

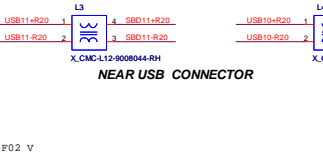
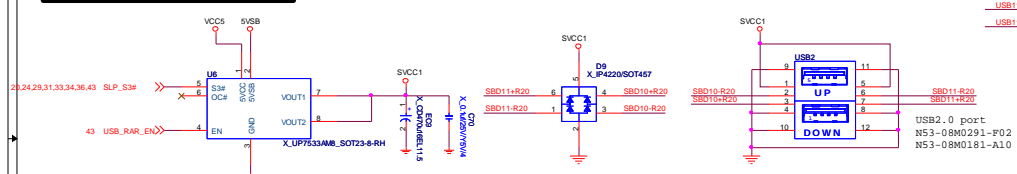


REAR PANEL USB/KB CONNECTOR FOR USB PORT 12,13



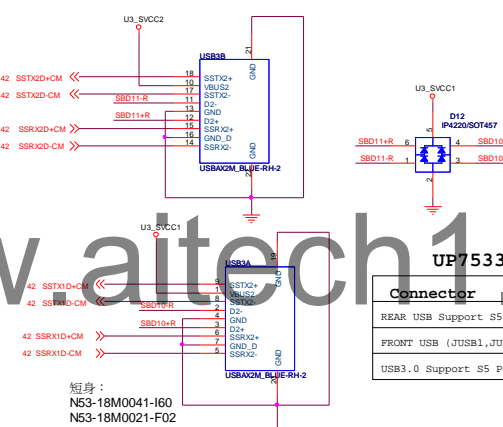
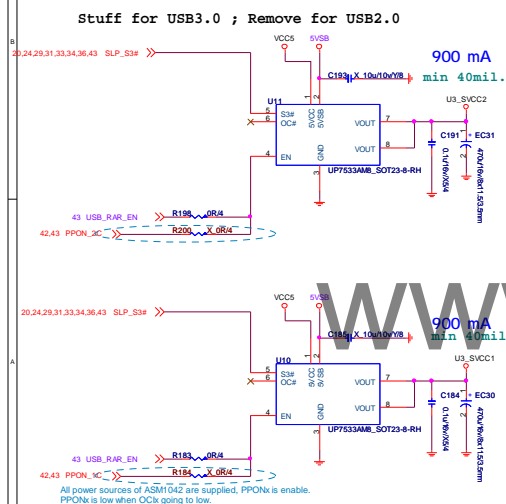
REAR POWER CONTROL

REAR PANEL USB/LAN CONNECTOR FOR USB PORT 10,11(Colay USB3.0) *option



USB3.0 POWER CONTROL

REAR PANEL USB CONNECTOR FOR USB PORT 10,11(Colay USB3.0)

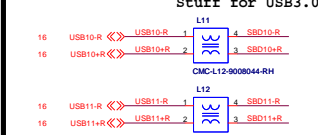


Stuff for USB2.0

USB11-R R212 X OR4 USB11-R20
USB11-R R211 X OR4 USB11-R20
USB10-R R210 X OR4 USB10-R20
USB10-R R205 X OR4 USB10-R20

NEAR REAR USB CONNECTOR

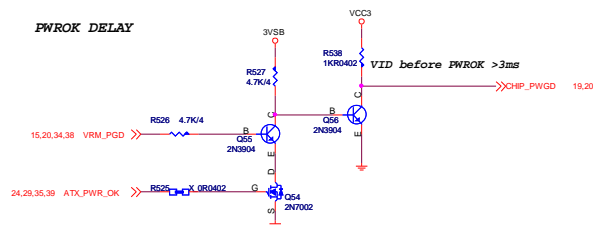
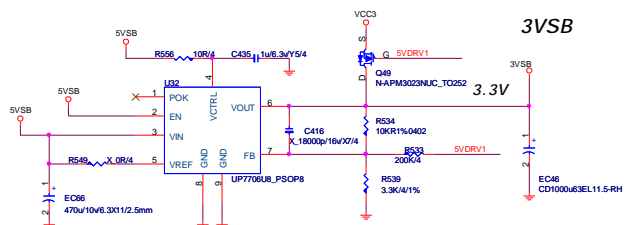
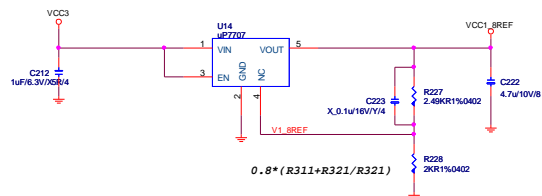
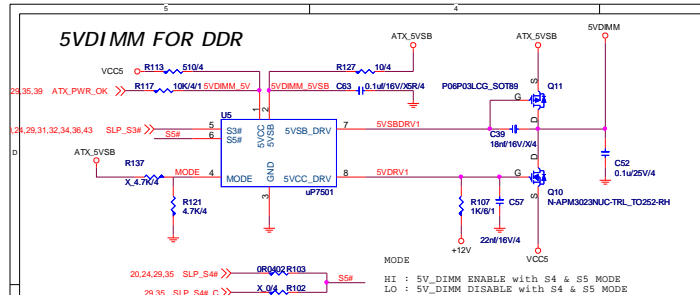
Stuff for USB3.0



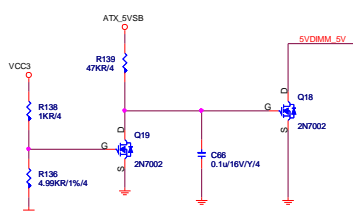
UP7533 ENABLE CONTROL

Connector	Power	GPIO Control
REAR USB Support S5 Power (KB/PS2/LAN)	SVCC1, SVCC2, SVCC3	USB_MODE
FRONT USB (JUSB1, JUSB2, JUSB3, JUSB4)	SVCC4, SVCC6, SVCC7	PCH_GP145
USB3.0 Support S5 Power	U3_SVCC1, U3_SVCC2	PCH_GP144

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Update from SLP S3# to VRM PGD

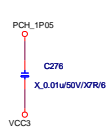
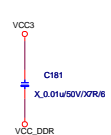
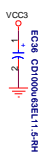
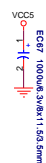
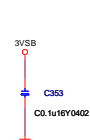
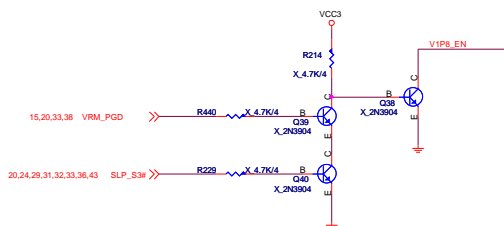


For power 700W solution
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.



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DDR3_1.5V

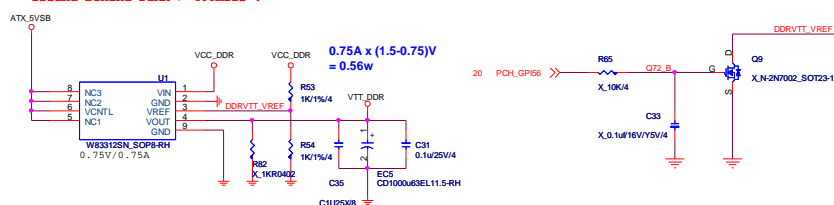
8A

21.65A



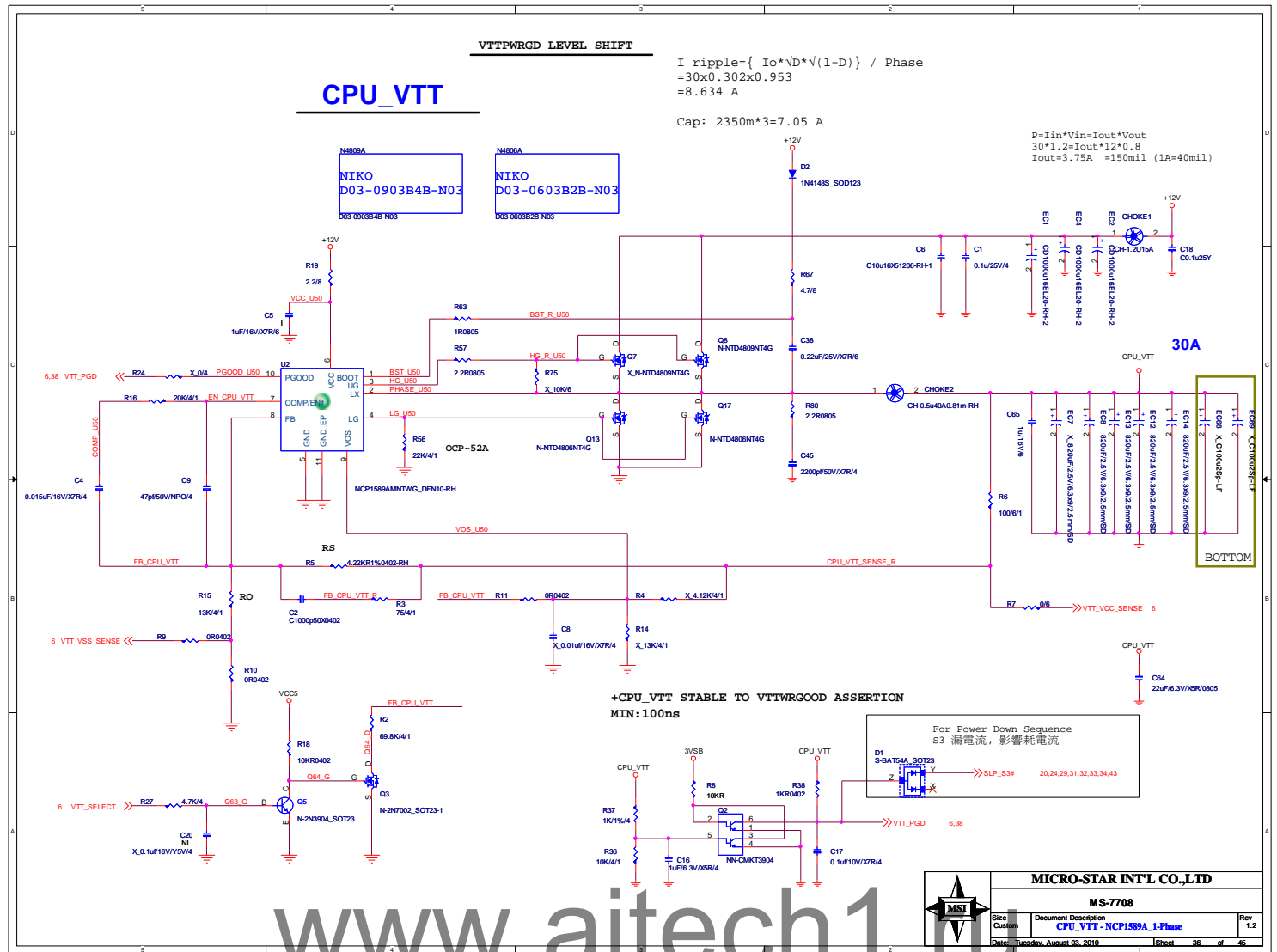
ATX_5VSB

VCC_DDR VCC_DDR $0.75A \times (1.5-0.75)V$



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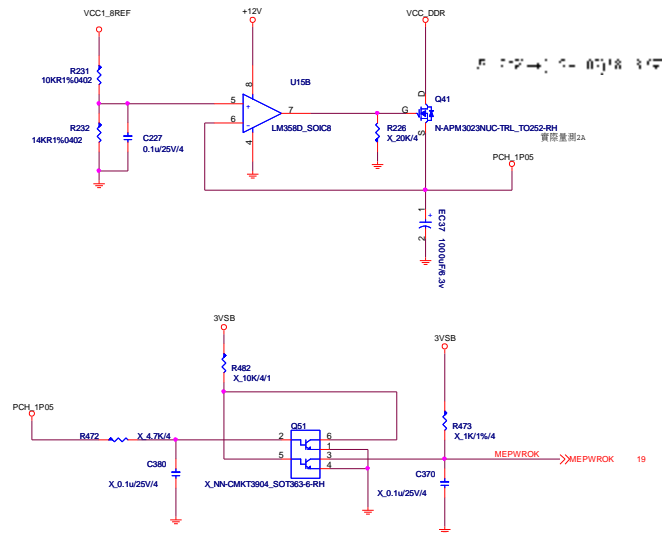
Size Custom	Document Description DDR POWER - NCP1587DR2G 1-Phase
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PCH Core

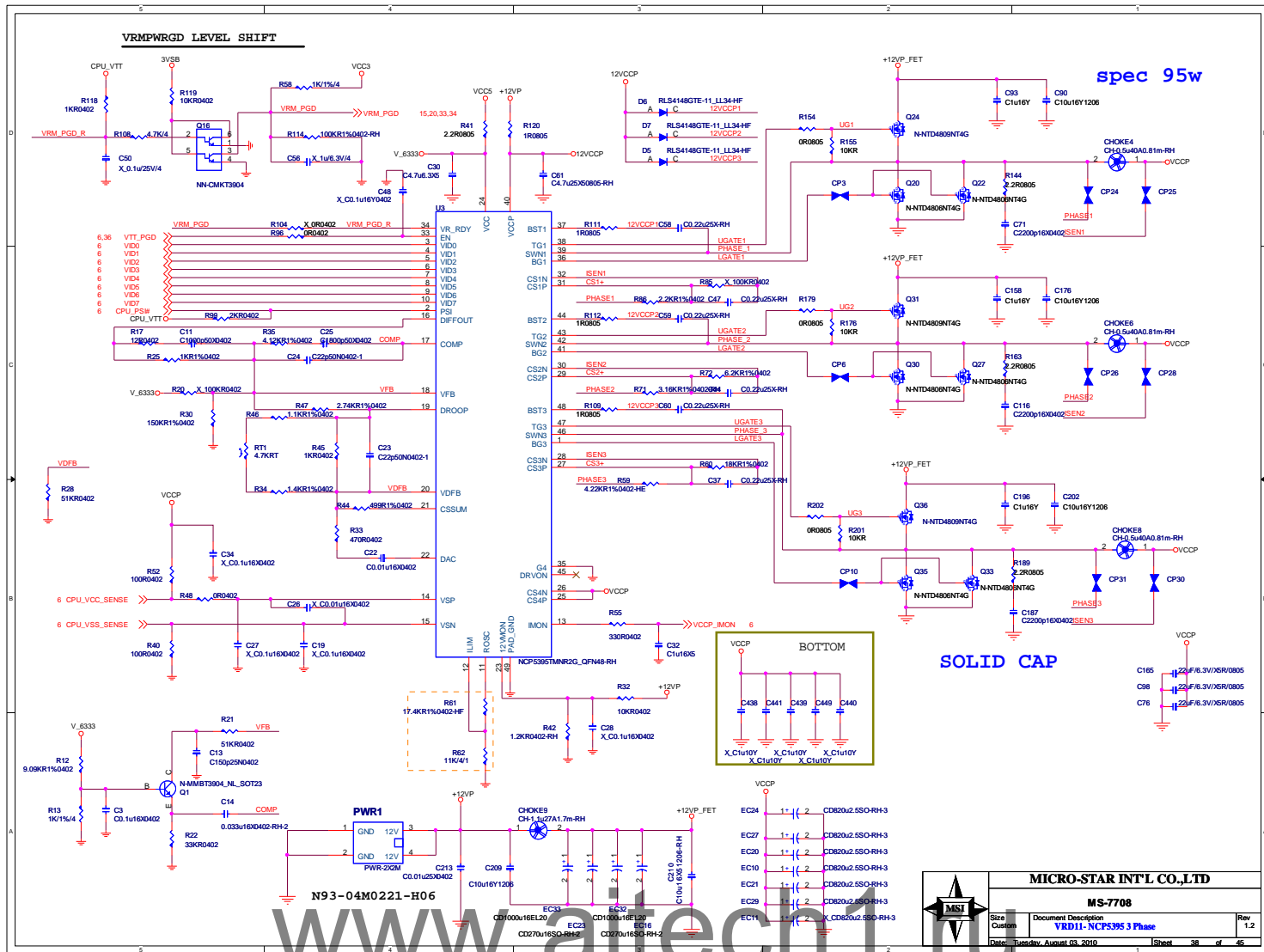
$$5.5A(PCH) + 2.5A(VCCME) = 8A$$



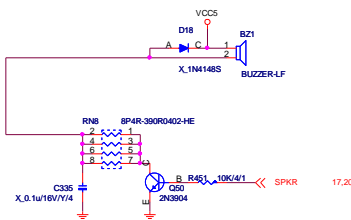
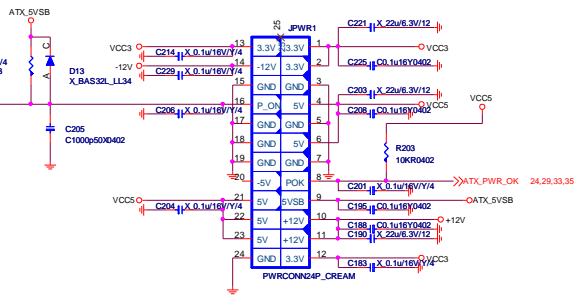
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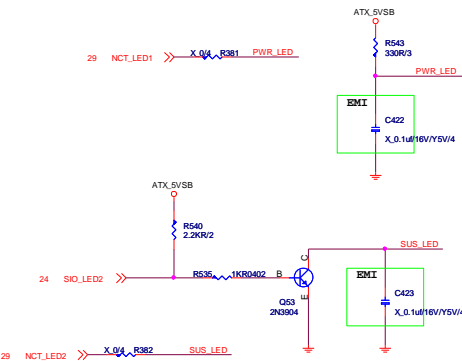
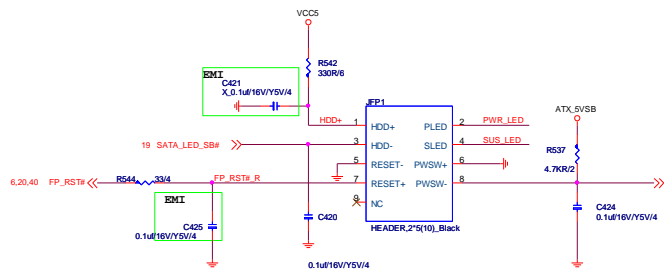


ATX POWER CONNECTOR



$R=390\ \Omega$
 $I=(5-0.2)/R=0.123\ A$
 $W=0.123A \times 5V=0.615W$ (夠耐電阻)
 $R=1/16W=0.062W$

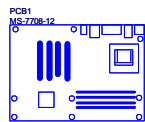
FRONT PANNEL



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PCB



P30-0770812-E55, 依頓 V
P30-0770812-G37, 精成

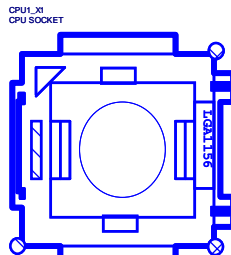


E31-0401634-K08



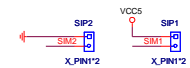
BAT-BCR2032P-RH

CPU SOCKET

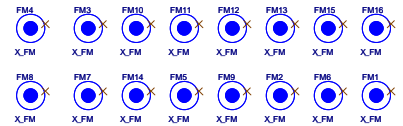


E21-7557010-F02

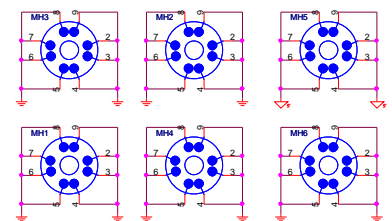
Simulation



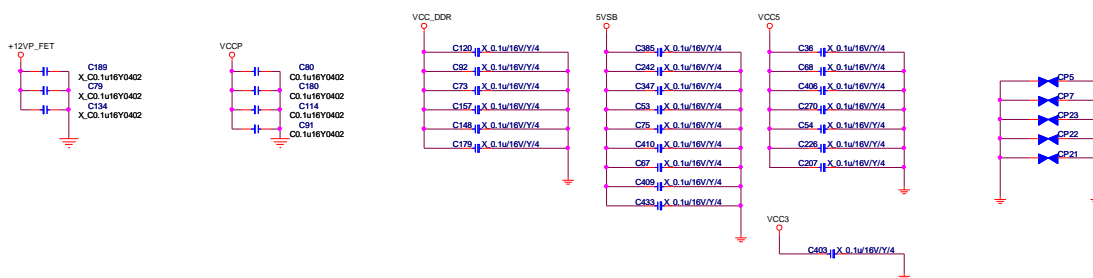
Optical Fiducial Marks-120



Mounting Holes



For EMI



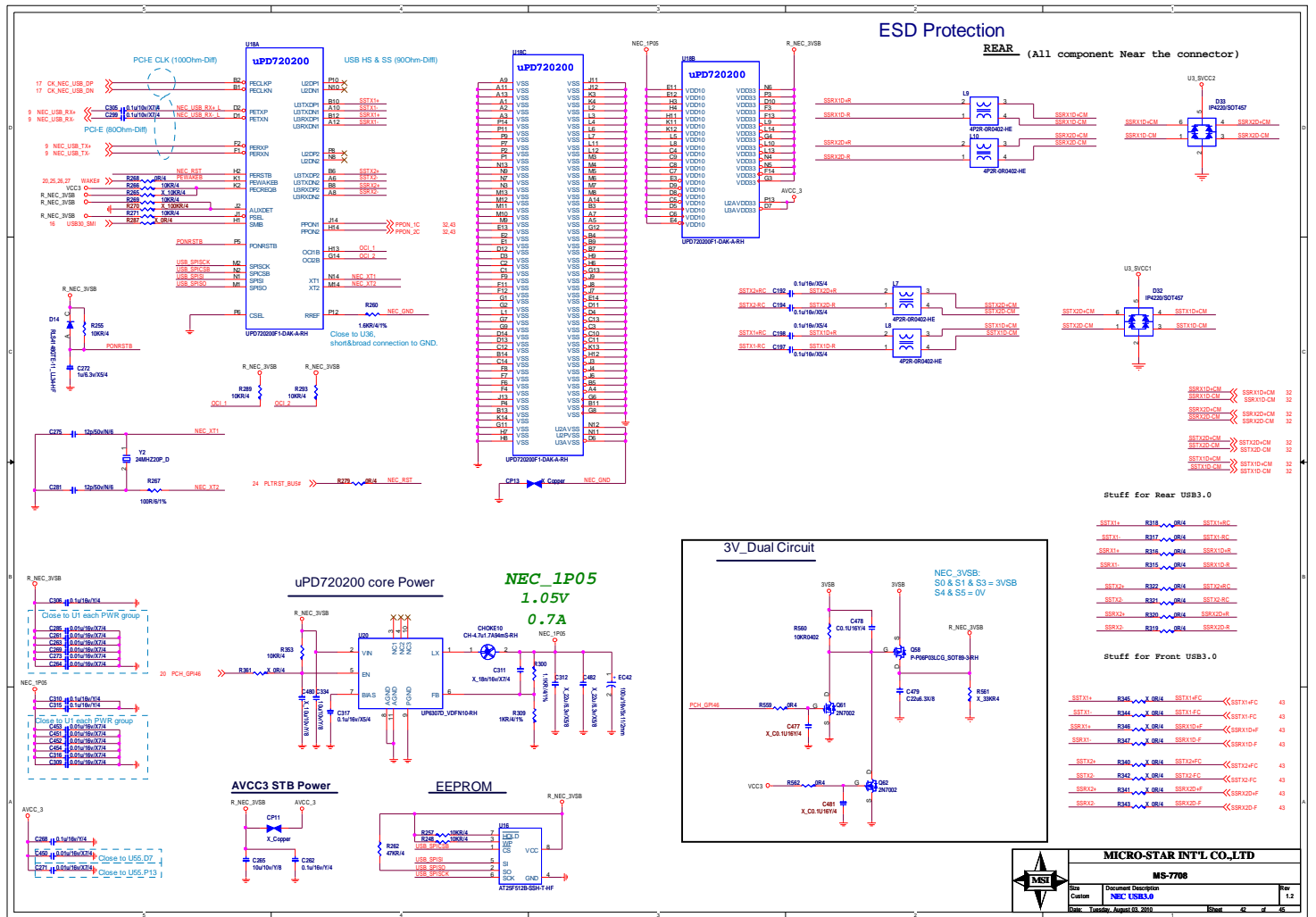
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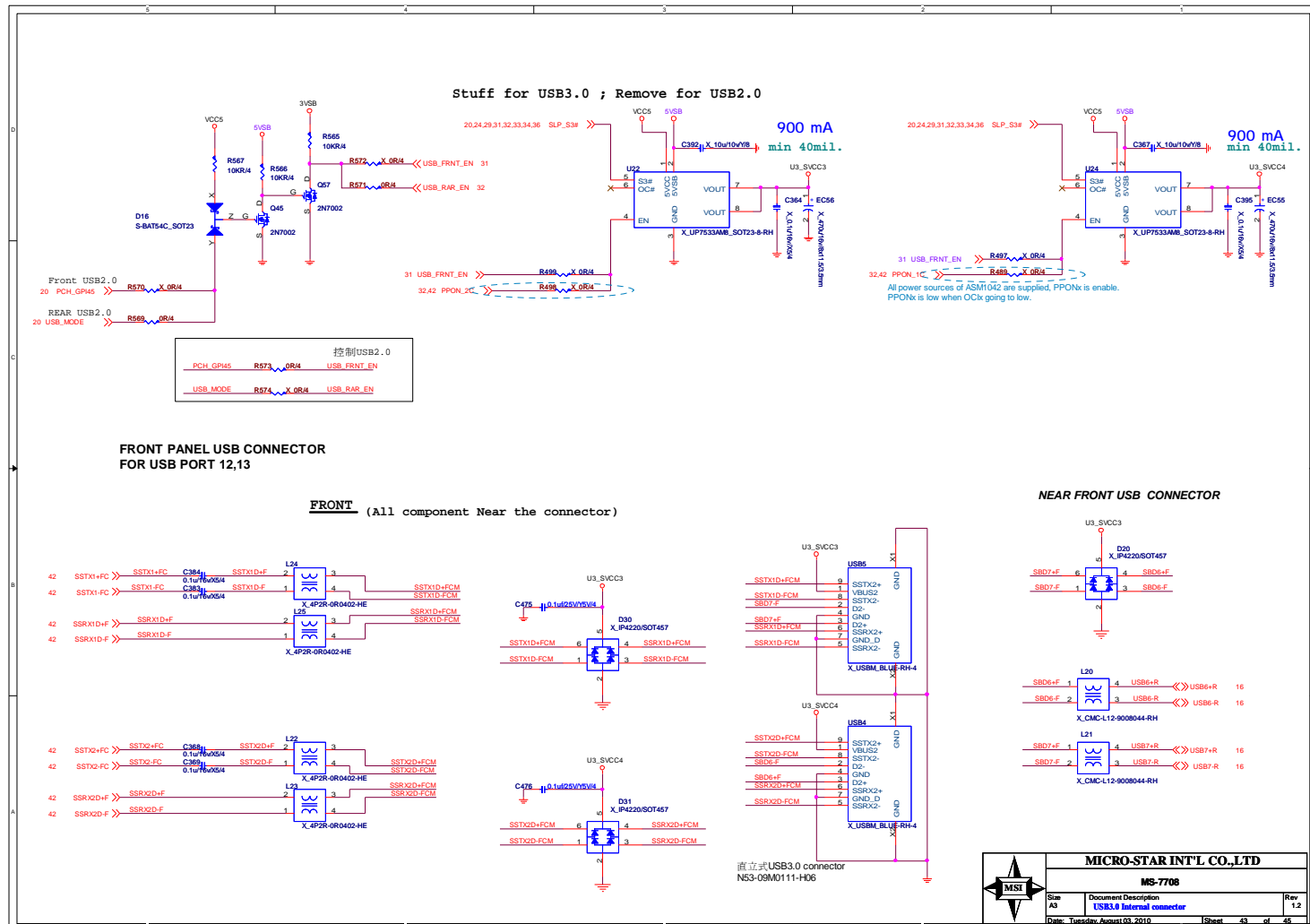
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